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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,034	11/17/2003	Louis M. Kindt	BUR920030115US1	1033

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1756	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,034	KINDT ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The disclosure is objected to because of the following informalities: page 2, line 7, "both type of masks", near bottom of page "masks projects"; page 12, middle of page, "114Finally" a period is missing.

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (6,787,460).

Lee et al. teach a method of forming a metal layer in an integrated circuit device, the method comprising: forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall; forming a selective electroplating mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective electroplating mask; and electroplating a metal on the exposed portion of the side wall.

And wherein forming a selective electroplating mask comprises forming the selective electroplating mask on the surface adjacent to the edge and on the side wall adjacent to the edge and not on the side wall beyond adjacent to the edge.

And wherein electroplating comprises electroplating the mental on the exposed portion of the side wall and on the bottom to fill the recess with the metal to beneath a level of the electroplating mask on the side wall.

Lee et al. also teach a barrier metal layer, such as tantalum nitride (TaN), is formed on the resultant structure in which the trench 13 and the hole 12 are formed. Then, a Cu seed layer 16 is formed thereon. Thereafter, a Cu layer 18 is deposited using an electroplating process to fill the hole 12.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al. (2004/0091789) in view of Lewis et al. (6,797,620) or Lee et al. (6,787,460).

The claimed invention is directed to a method for controlling the linewidth in an extreme ultraviolet lithography (EUVL) mask, and the mask structure, comprising: a multilayer (ML) reflective layer formed on a starting substrate; a buffer layer formed on said reflective layer; an absorber layer formed on said buffer layer, wherein said absorber layer includes an electrochemically deposited additive material on exposed sidewalls during initial etching thereof;

the method comprising: electrochemically depositing an additive material on exposed sidewalls of an etched absorber layer of the mask, wherein the top of said etched absorber layer remains covered by a hardmask used during the etching of said etched absorber layer; and

wherein a buffer layer beneath said etched absorber layer is resistant to the electrochemical deposition of said additive material thereupon.

And further comprising: removing said hardmask, and etching said buffer layer with a resulting pattern defined by said absorber first layer plus said additive material, wherein: said absorber layer comprises an optically opaque layer; and said buffer layer is disposed between said absorber layer and a multilayer (ML) reflective layer underneath said buffer layer.

Han et al. teach a method for making a reflective mask useful for transferring a pattern to a semiconductor substrate using extreme ultraviolet (EUV) radiation comprising: providing a mask substrate; forming a lower multilayer reflective stack over the mask substrate; forming an etch stop layer over the lower multilayer reflective stack; forming an upper multilayer reflective stack on the etch stop layer; and etching an opening through the upper multilayer reflective stack to expose the etch stop layer.

And wherein the etch stop layer comprises a material selected from a group consisting of chromium, ruthenium, chrome oxide, chrome nitride, boron carbide, zirconium, tantalum oxide, tantalum nitride, tantalum silicon nitride.

The teachings of Han et al. differ from those of the applicant in that the applicant teaches electrochemically depositing an additive material on exposed sidewalls of an etched absorber layer of the mask.

Lewis et al. teach a method for processing a substrate having a field and an aperture comprising a bottom and sidewalls formed therein, the method comprising: depositing a nucleation layer on the bottom and sidewalls of the aperture; depositing a nucleation inhibiting material selected from the group of silicon, silicon dioxide, aluminum, aluminum oxide, tantalum, tantalum oxide, nickel, nickel oxide, titanium, titanium oxide, tungsten, tungsten oxide, and combinations thereof, on at least one of the field of the substrate and an upper portion of the

sidewalls of the aperture; and depositing a conductive material on the nucleation layer and the nucleation inhibiting material by an electrochemical deposition technique.

Lee et al. teach a method of forming a metal layer in an integrated circuit device, the method comprising: forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall; forming a selective electroplating mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective electroplating mask; and electroplating a metal on the exposed portion of the side wall.

And wherein forming a selective electroplating mask comprises forming the selective electroplating mask on the surface adjacent to the edge and on the side wall adjacent to the edge and not on the side wall beyond adjacent to the edge.

And wherein electroplating comprises electroplating the mental on the exposed portion of the side wall and on the bottom to fill the recess with the metal to beneath a level of the electroplating mask on the side wall.

Lee et al. also teach a barrier metal layer, such as tantalum nitride (TaN), is formed on the resultant structure in which the trench 13 and the hole 12 are formed. Then, a Cu seed layer 16 is formed thereon. Thereafter, a Cu layer 18 is deposited using an electroplating process to fill the hole 12.

It would have been obvious to one having ordinary skill in the art to take the teachings of Han et al. and combine them with the teachings of Lewis et al. or Lee et al. in order to make the claimed invention because the applicant is using a known technique to increase sidewall width.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
08/11/05